

MT8305M5

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = 30V$
- $I_D = 100A$
- $R_{DS(ON)} = 2.1 m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} = 2.6 m\Omega @ V_{GS} = 4.5V$

Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.
- PDFN5x6-8L Package

Applications

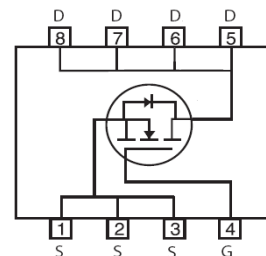
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



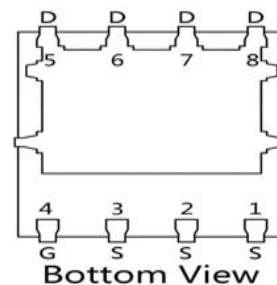
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Absolute Maximum Ratings $(T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	100	A
Current	I_D	75	A
Pulsed Drain Current ²	I_{DM}	230	A
Continuous Drain Current	I_{DSM}	27	A
Current	I_{DSM}	21	A
Avalanche Current	I_{AR}	40	A
Repetitive avalanche energy $L=0.3mH^3$	E_{AR}	180	mJ
Power Dissipation	P_D	85	W
Power Dissipation	P_{DSM}	55	W
Power Dissipation	P_{DSM}	2.5	W
Power Dissipation	P_{DSM}	1.5	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient	$t \leq 10s$	$R_{\theta JA}$	14	17	$^{\circ}C/W$
Maximum Junction-to-Ambient	Steady-State		40	55	$^{\circ}C/W$
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.85	1.5	$^{\circ}C/W$

Electrical Characteristics ($T_J=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu A, V_{GS}=0V$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$ $T_J=55^{\circ}C$			1 50	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0V, V_{GS}= \pm 16V$			10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.5	1.85	2.2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance ^a	$V_{GS}=10V, I_D=20A$ $T_J=125^{\circ}C$		2.1 2.8	2.4 3.4	$m\Omega$
		$V_{GS}=4.5V, I_D=20A$		2.6	3.2	$m\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=20A$		130		S
V_{SD}	Diode Forward Voltage	$I_S=1A, V_{GS}=0V$		0.67	1	V
I_S	Maximum Body-Diode Continuous Current				100	A
DYNAMIC PARAMETERS^b						
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=15V, f=1MHz$	-	2335	-	pF
C_{oss}	Output Capacitance		-	650	-	pF
C_{rss}	Reverse Transfer Capacitance		-	335	-	pF
R_g	Gate resistance	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	1	2	3	Ω
SWITCHING PARAMETERS						
$Q_g(10V)$	Total Gate Charge	$V_{GS}=10V, V_{DS}=15V, I_D=20A$	35	40	46	nC
$Q_g(4.5V)$	Total Gate Charge		15	23	30	nC
Q_{gs}	Gate Source Charge			10		nC
Q_{gd}	Gate Drain Charge			16		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10V, V_{DS}=15V, R_L=0.75\Omega, R_{GEN}=3\Omega$		10		ns
t_r	Turn-On Rise Time			6.5		ns
$t_{D(off)}$	Turn-Off DelayTime			45.5		ns
t_f	Turn-Off Fall Time			17.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20A, dI/dt=500A/\mu s$		29	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20A, dI/dt=500A/\mu s$		13.5		nC

Notes:

1. Surface Mounted on 1" x 1" FR4 Board, $t \leq 10$ Sec.
2. Pulse width limited by maximum junction temperature.
3. The test condition is $T_J=25^{\circ}C, V_{DD}=30V, V_{GS}=10V, L=0.1mH, R_G=25\Omega, I_{AS}=50A$.
 - a. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 - b. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

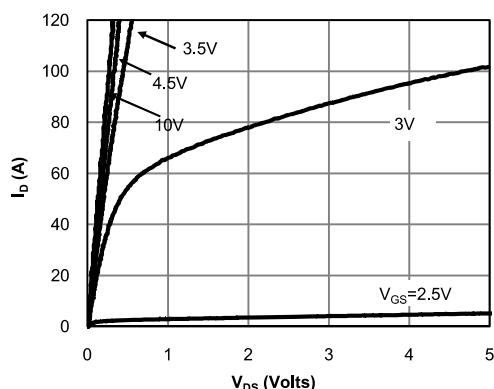


Fig 1: On-Region Characteristics (Note E)

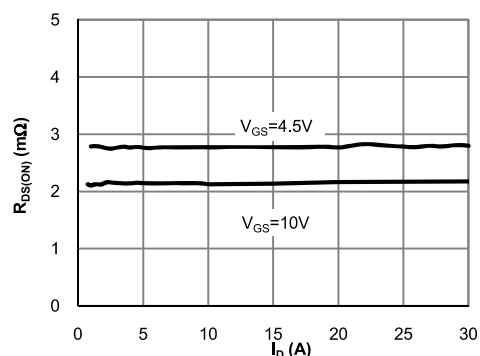
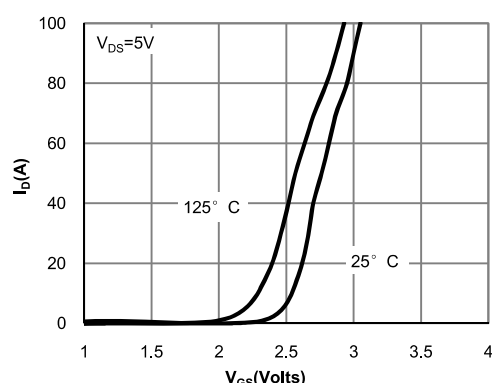


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

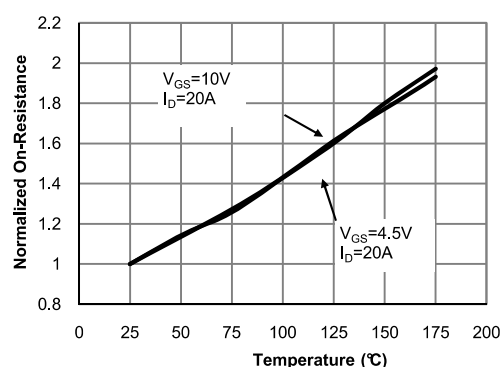


Figure 4: On-Resistance vs. Junction Temperature (Note E)

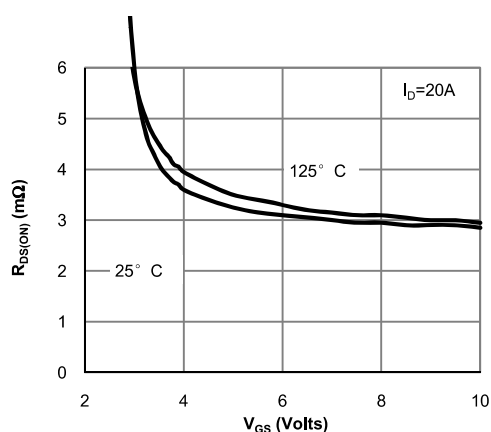


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

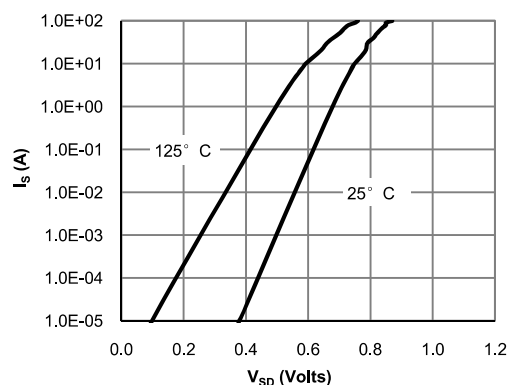
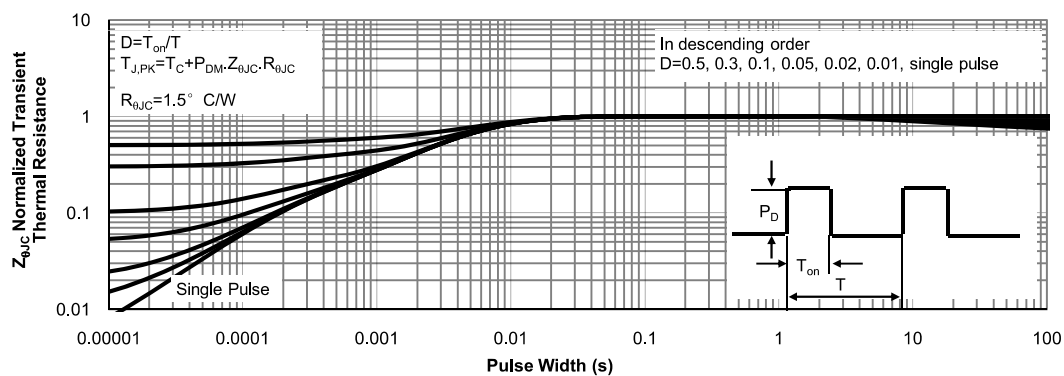
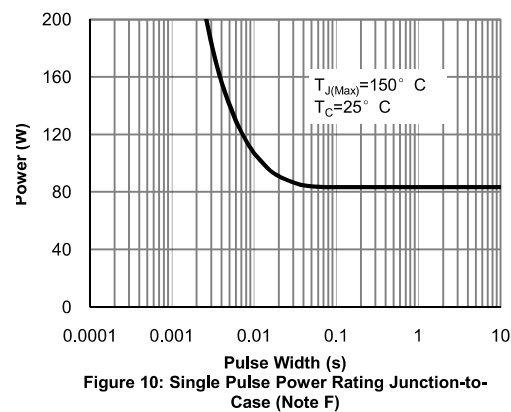
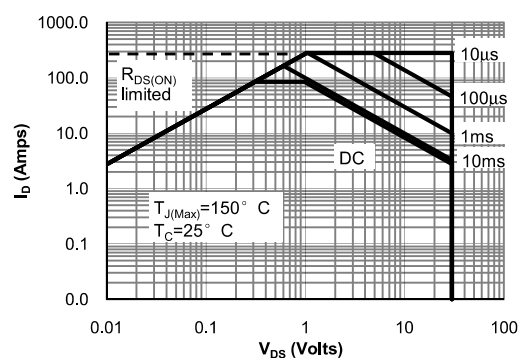
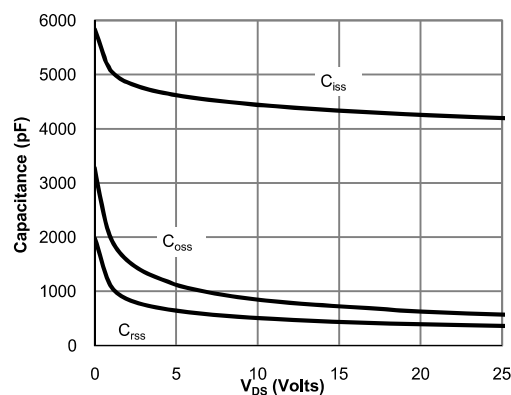
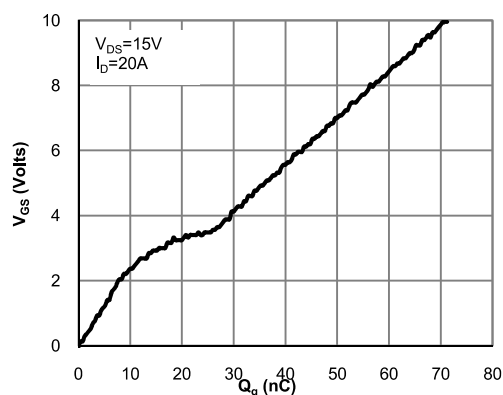


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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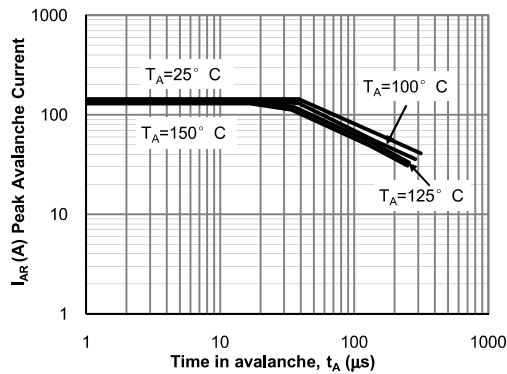


Figure 12: Single Pulse Avalanche capability (Note C)

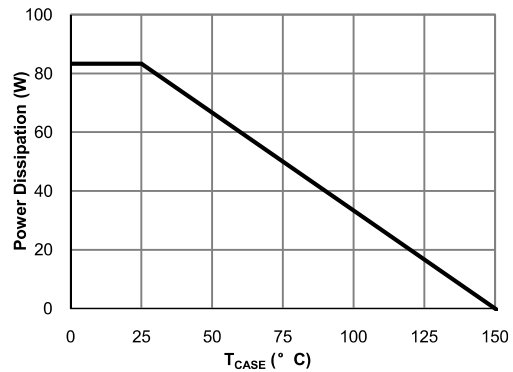


Figure 13: Power De-rating (Note F)

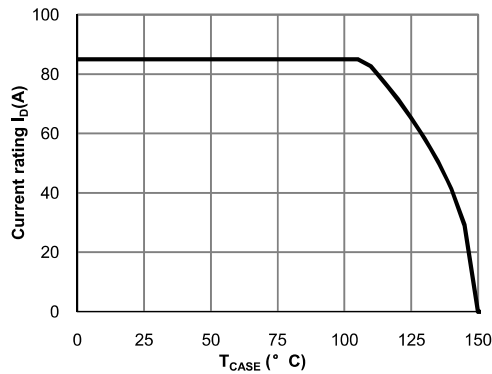


Figure 14: Current De-rating (Note F)

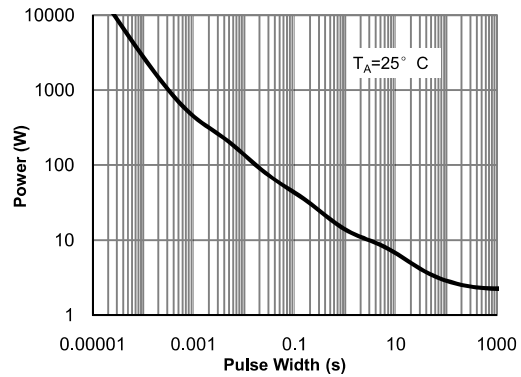


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

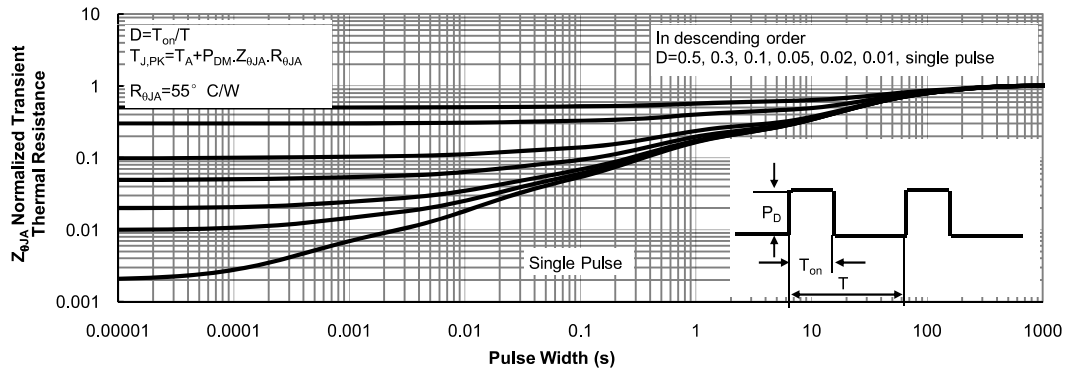
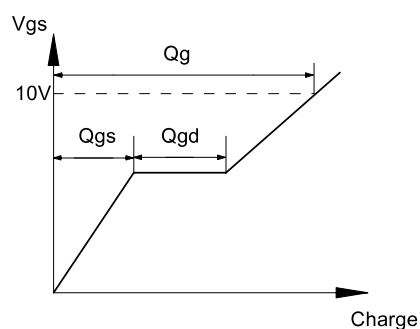
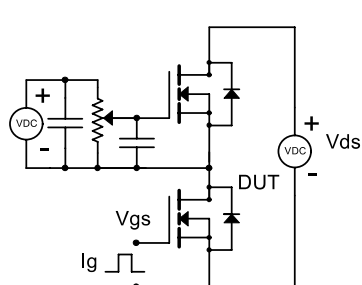
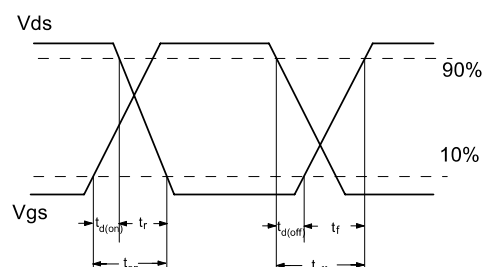
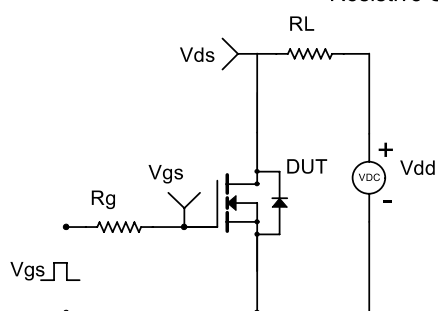


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

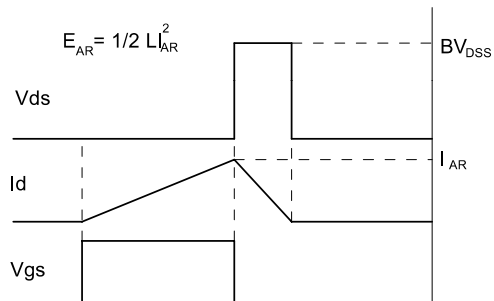
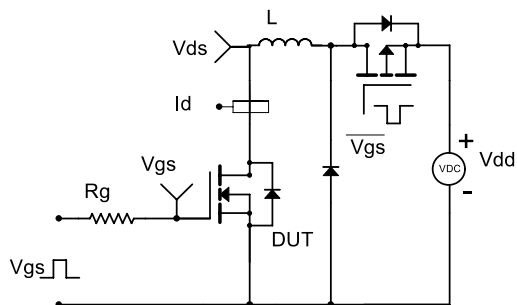
Gate Charge Test Circuit & Waveform



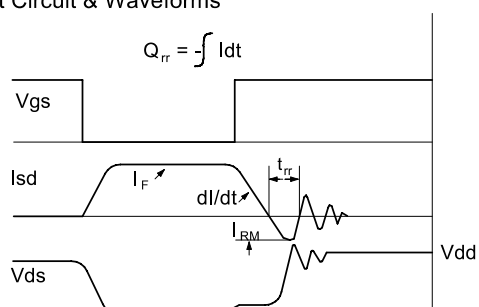
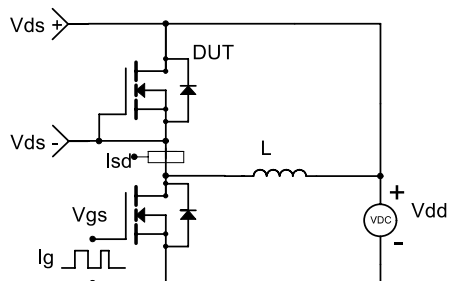
Resistive Switching Test Circuit & Waveforms



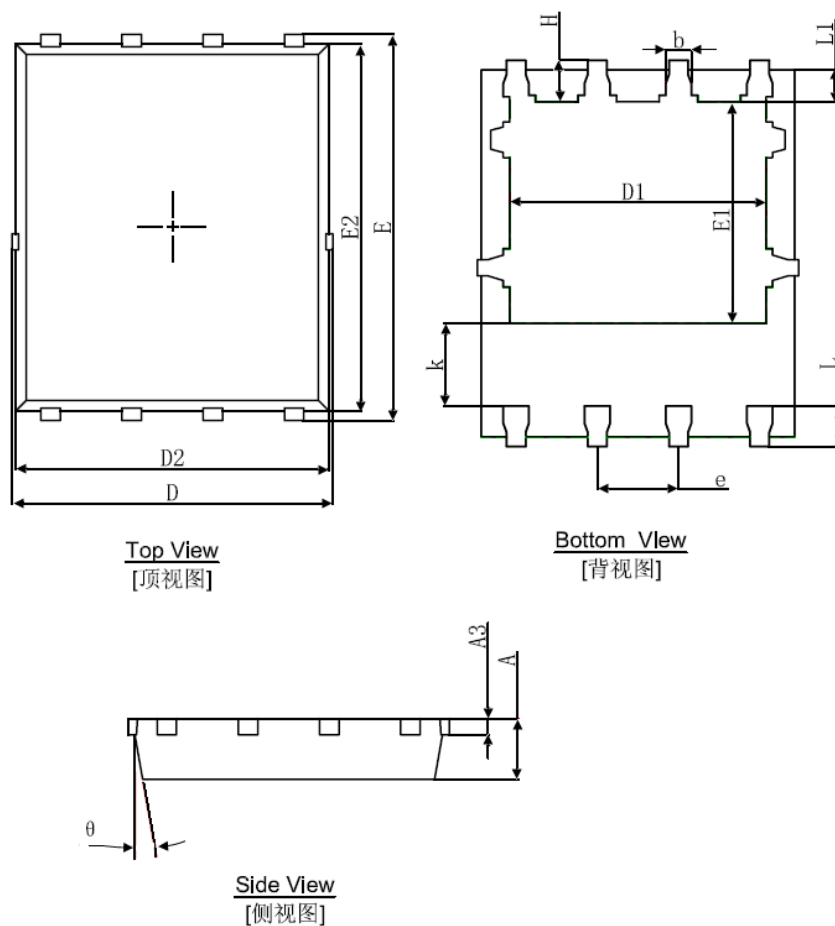
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



PDFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
K	1.190	1.390	0.047	0.055
b	0.035	0.450	0.014	0.018
e	1.270(TYP.)		0.050(TYP.)	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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