

MT4420

N-Channel PowerTrench[®] MOSFET 30V, 15A, 6.8mΩ



MT Semiconductor[®]

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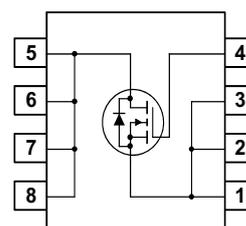
General Description

This N-Channel MOSFET has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(on)}$ and fast switching speed.

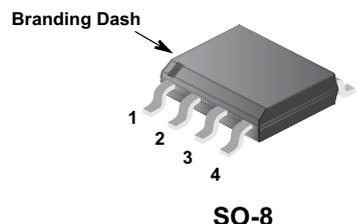
Features

- $R_{DS(on)} = 6.8m\Omega$, $V_{GS} = 10V$, $I_D = 15A$
- $R_{DS(on)} = 9.3m\Omega$, $V_{GS} = 4.5V$, $I_D = 14A$
- Low gate charge
- High performance trench technology for extremely low $R_{DS(on)}$
- High power and current handling capability
- RoHS compliant

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_A = 25^\circ C$, $V_{GS} = 10V$, $R_{\theta JA} = 50^\circ C/W$)	15	A
	Continuous ($T_A = 25^\circ C$, $V_{GS} = 4.5V$, $R_{\theta JA} = 50^\circ C/W$)	14	A
	Pulsed	110	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	196	mJ
P_D	Power dissipation	2.5	W
	Derate above $25^\circ C$	20	mW/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2b)	125	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT4420	MT4420	SO-8	330mm	12mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1.2	-	2.5	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 15\text{A}$, $V_{GS} = 10\text{V}$	-	6.8	8.5	m Ω
		$I_D = 14\text{A}$, $V_{GS} = 4.5\text{V}$	-	9.3	12	
		$I_D = 15\text{A}$, $V_{GS} = 10\text{V}$, $T_J = 150^\circ\text{C}$	-	7.8	10.1	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	1525	-	pF
C_{OSS}	Output Capacitance		-	490	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	300	-	pF
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}$, $f = 1\text{MHz}$	0.6	2.4	4.2	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	50	67	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V	-	28	36	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V	-	2.5	3.2	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 15\text{V}$ $I_D = 15\text{A}$ $I_g = 1.0\text{mA}$	-	7.0	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	4.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	11	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 15\text{V}$, $I_D = 14\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 6.2\Omega$	-	-	6.8	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	27	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	8.6	-	ns
t_f	Fall Time		-	24	-	ns
t_{OFF}	Turn-Off Time		-	-	12.6	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 15\text{A}$	-	-	1.25	V
		$I_{SD} = 2.1\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 15\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	29	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 15\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	15	nC

Notes:

1: Starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $I_{AS} = 19.8\text{A}$, $V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$.

2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a) $50^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper.

b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

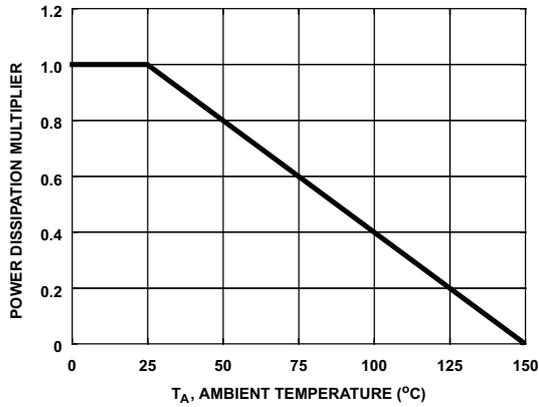


Figure 1. Normalized Power Dissipation vs Ambient Temperature

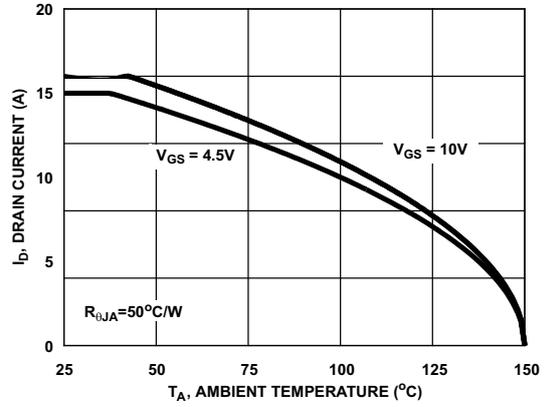


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

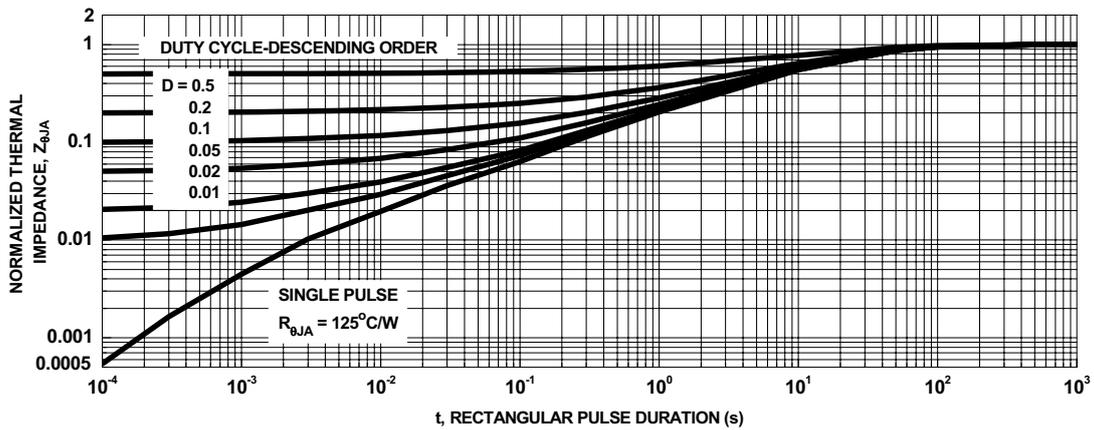


Figure 3. Normalized Maximum Transient Thermal Impedance

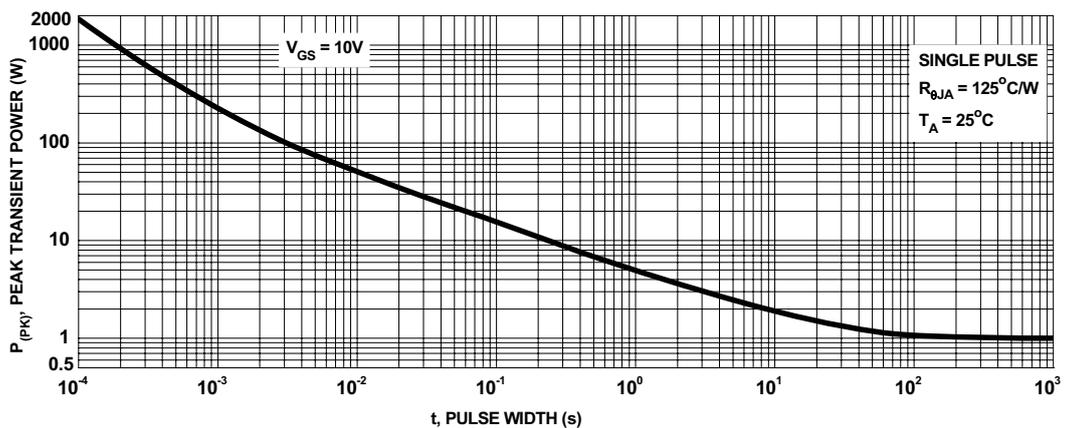
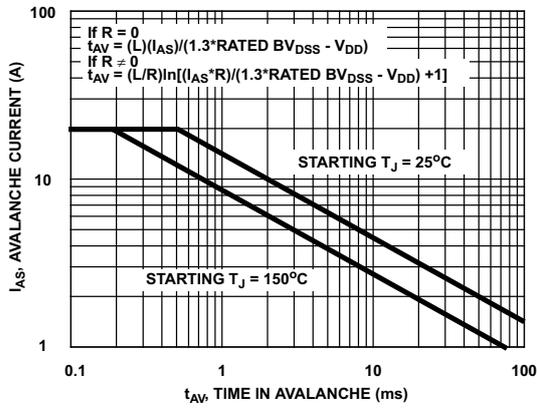


Figure 4. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
Figure 5. Unclamped Inductive Switching Capability

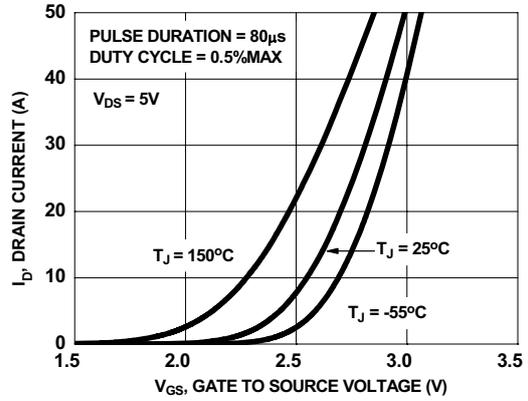


Figure 6. Transfer Characteristics

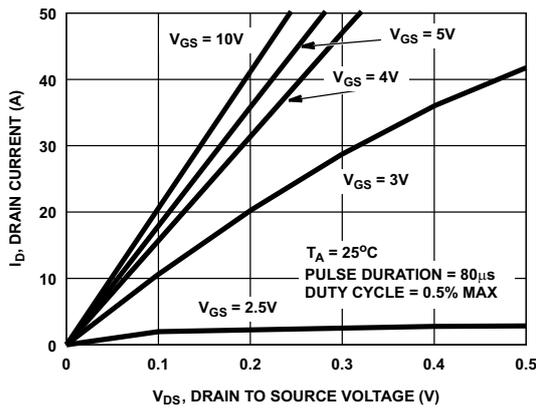


Figure 7. Saturation Characteristics

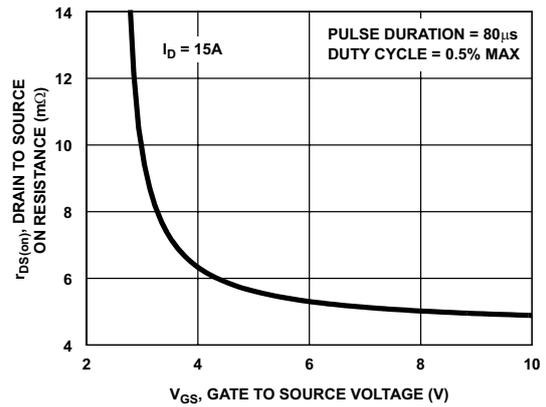


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

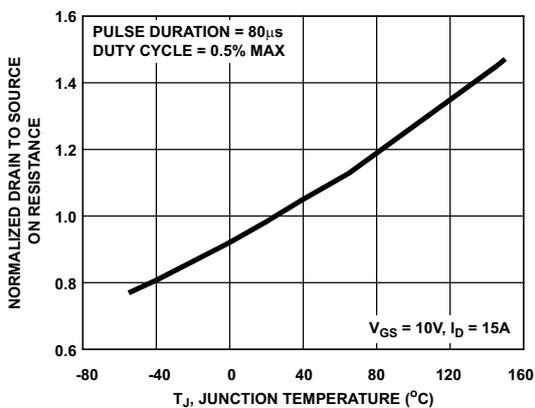


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

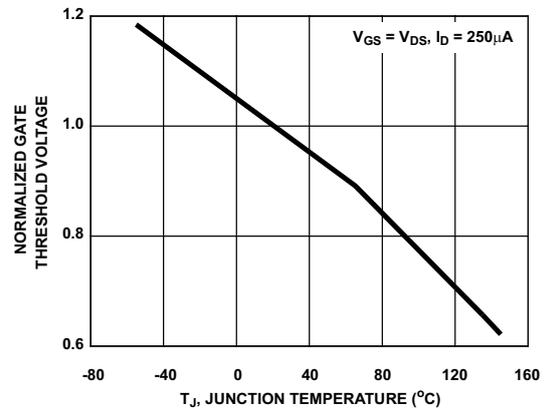


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

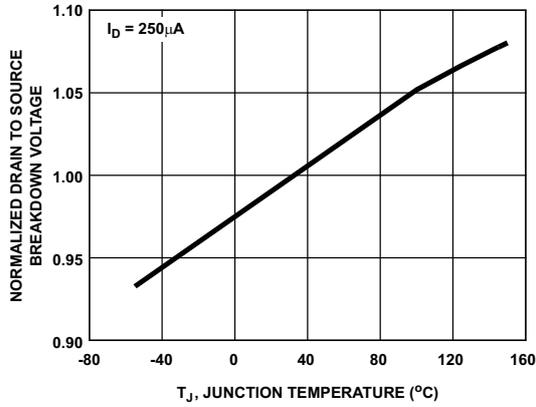


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

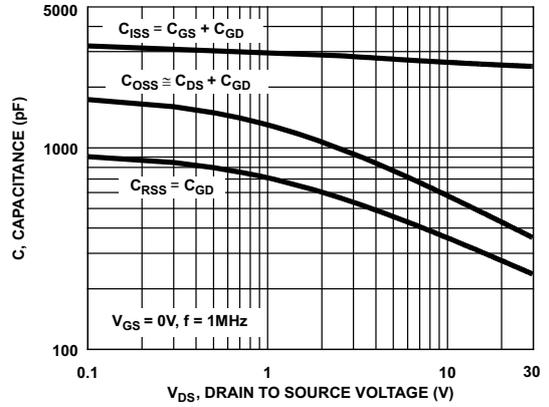


Figure 12. Capacitance vs Drain to Source Voltage

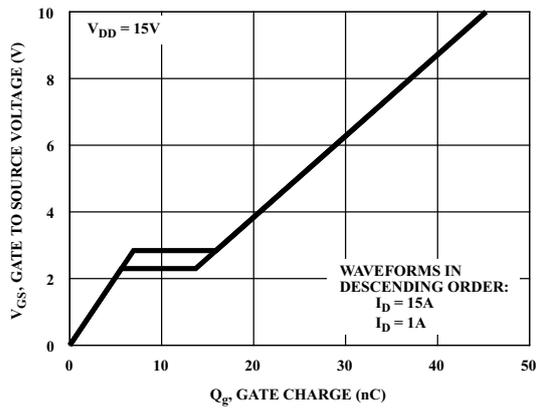


Figure 13. Gate Charge Waveforms for Constant Gate Currents

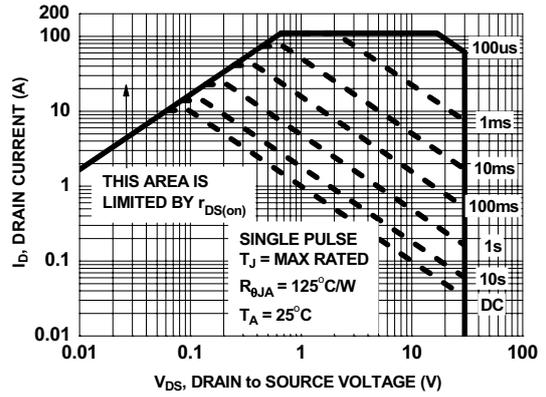


Figure 14. Forward Bias Safe Operating Area

Test Circuits and Waveforms

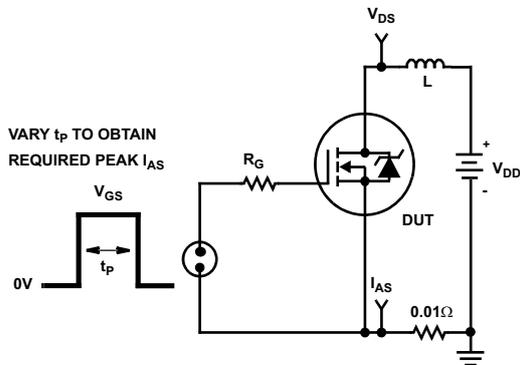


Figure 15. Unclamped Energy Test Circuit

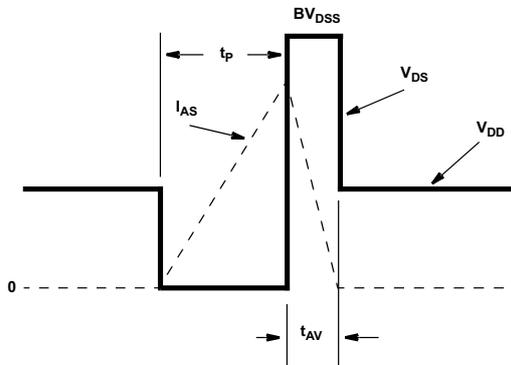


Figure 16. Unclamped Energy Waveforms

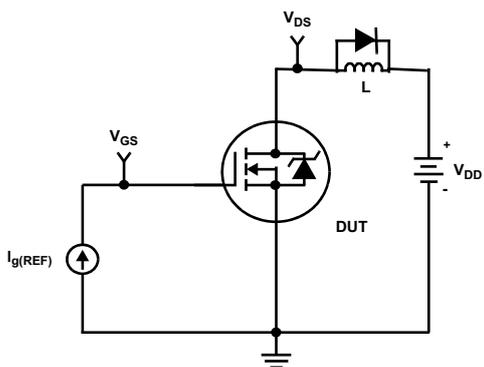


Figure 17. Gate Charge Test Circuit

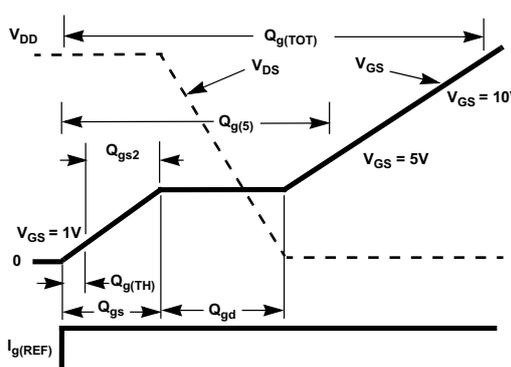


Figure 18. Gate Charge Waveforms

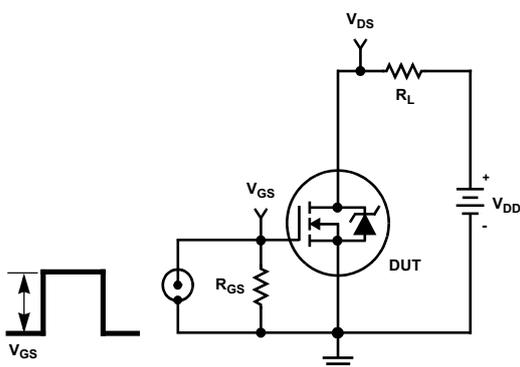


Figure 19. Switching Time Test Circuit

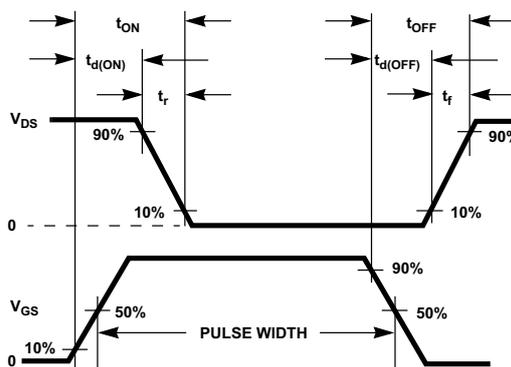
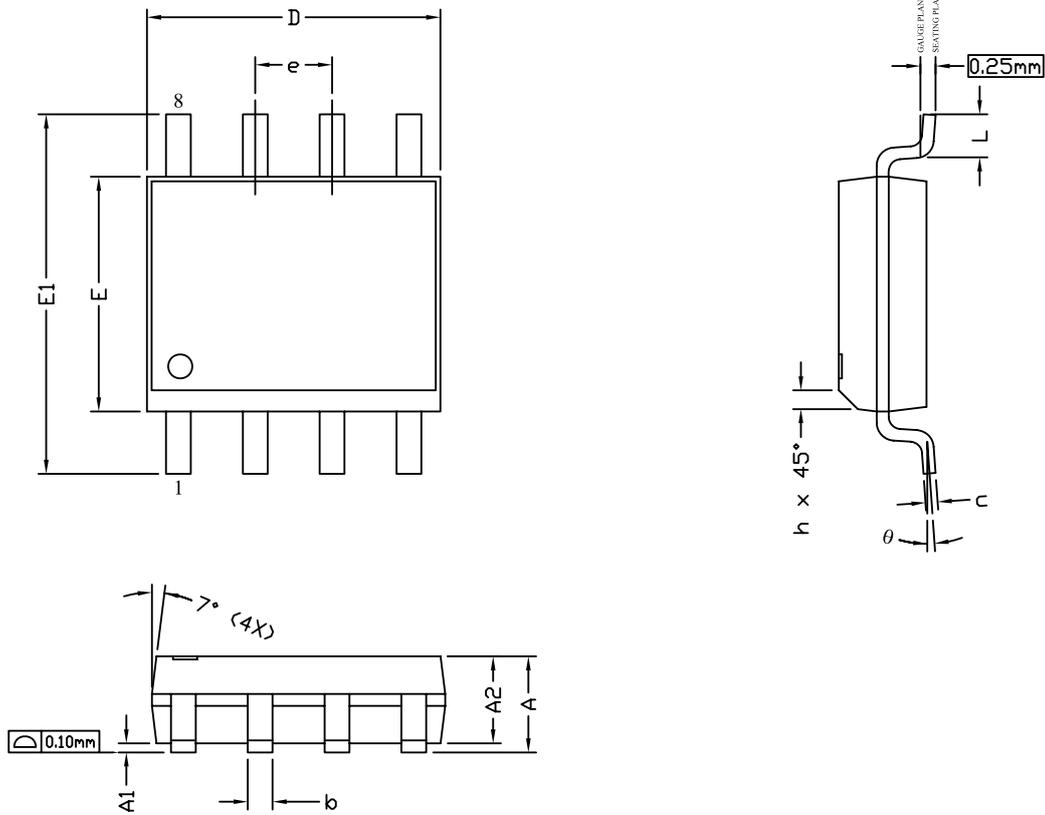


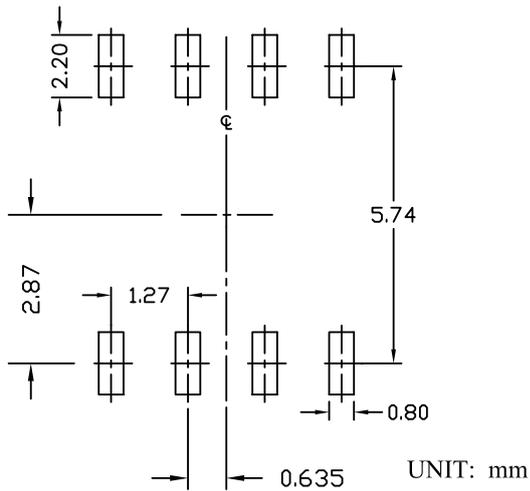
Figure 20. Switching Time Waveforms

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Version	rev H

S08 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	---	0.25	0.004	---	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	---	0.51	0.012	---	0.020
c	0.17	---	0.25	0.007	---	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	---	0.50	0.010	---	0.020
L	0.40	---	1.27	0.016	---	0.050
θ	0°	---	8°	0°	---	8°

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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