

# MT36P50S

## P-Channel Enhancement Mode Field Effect Transistor

### Product Summary

- $V_{DS} = -60V$
- $I_D = -50A$  ( $V_{GS} = -10V$ )
- $R_{DS(ON)} 23m\Omega$  @  $V_{GS} = -10V$

### Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

### Applications

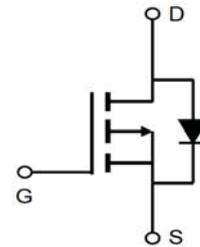
- Power Switching Application
- Hard switched and high frequency circuit
- UPS
- Load Switch



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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



TO-252-2L

### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-50	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	-35	A
Pulsed Drain Current	$I_{DM}$	-150	A
Maximum Power Dissipation	$P_D$	95	W
Derating factor		0.76	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	722	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.31	$^\circ C/W$
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### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT36P50S	MT36P50S	TO-252-2L	-	-	2500

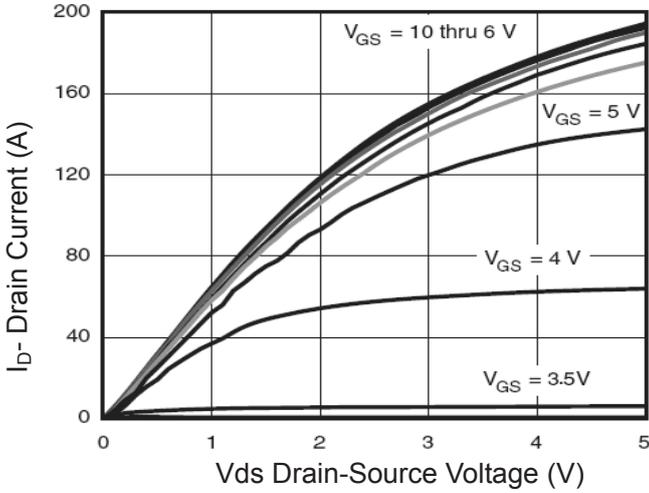
**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-2.0	-2.6	-3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	23	28	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-10V, I_D=-20A$	-	25	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{iss}$	$V_{DS}=-25V, V_{GS}=0V,$ $F=1.0MHz$	-	6460	-	PF
Output Capacitance	$C_{oss}$		-	719	-	PF
Reverse Transfer Capacitance	$C_{rSS}$		-	535	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=1.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	15	-	nS
Turn-on Rise Time	$t_r$		-	17	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	40	-	nS
Turn-Off Fall Time	$t_f$		-	45	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-30, I_D=-20A,$ $V_{GS}=-10V$	-	75	-	nC
Gate-Source Charge	$Q_{gs}$		-	16	-	nC
Gate-Drain Charge	$Q_{gd}$		-	19	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=-20A$	-	-	-1.2	V
Diode Forward Current	$I_S$		-	-	-50	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = -20A$	-	50	-	nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = -100A/\mu s$ (Note 3)	-	59	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

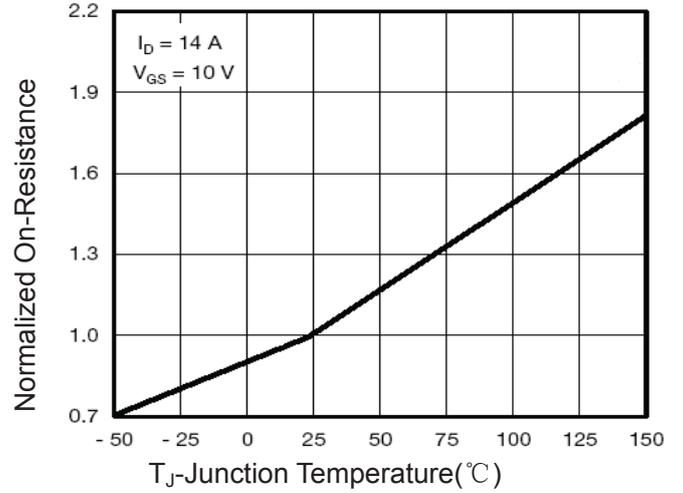
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^\circ\text{C}, V_{DD}=-30V, V_G=-10V, L=1mH, R_g=25\Omega, I_{AS}=38A$

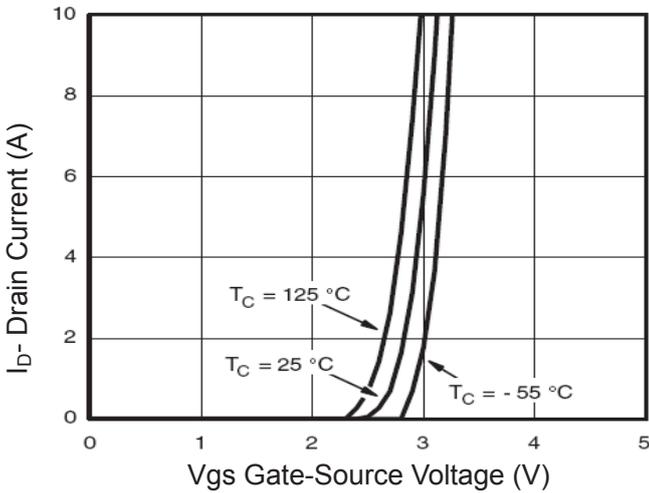
### Characteristics Curve



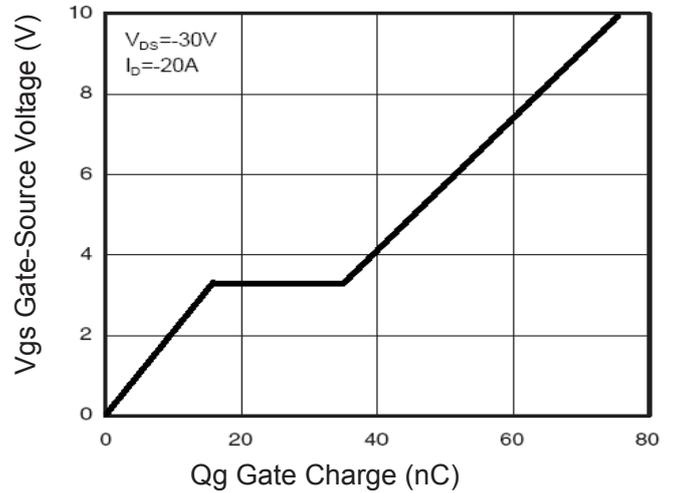
**Figure 1 Output Characteristics**



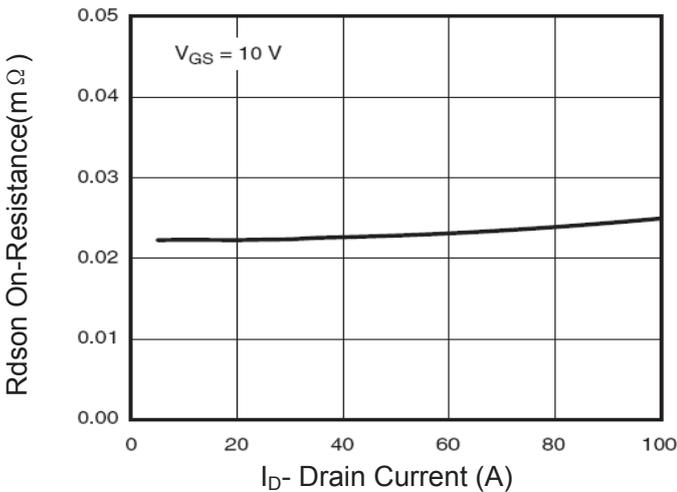
**Figure 4 Rdson-Junction Temperature**



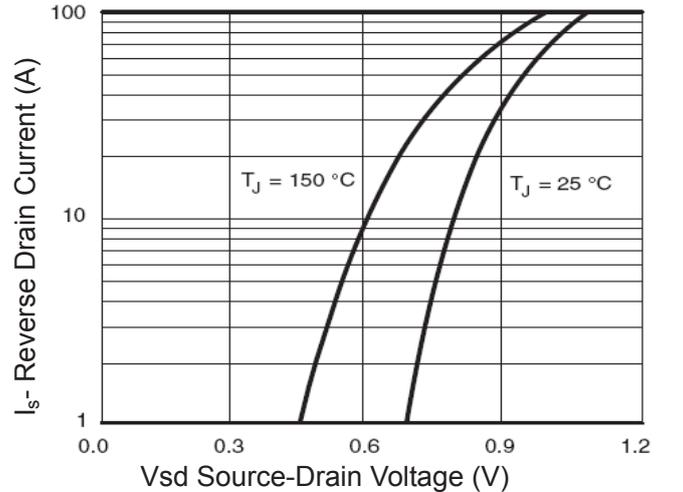
**Figure 2 Transfer Characteristics**



**Figure 5 Gate Charge**



**Figure 3 Rdson- Drain Current**



**Figure 6 Source- Drain Diode Forward**

## Characteristics Curve

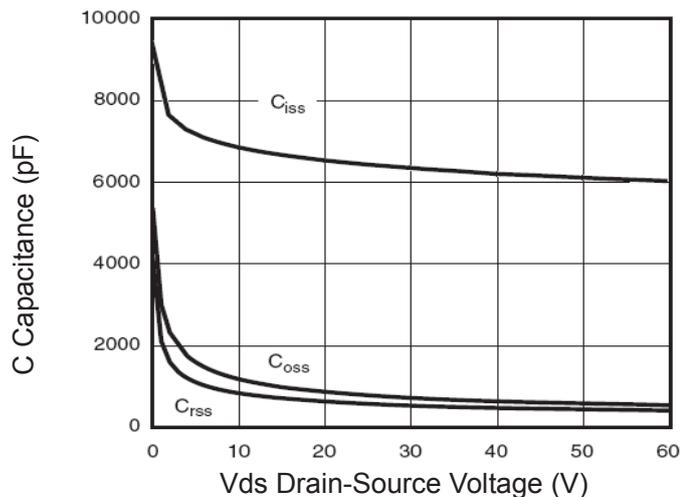


Figure 7 Capacitance vs Vds

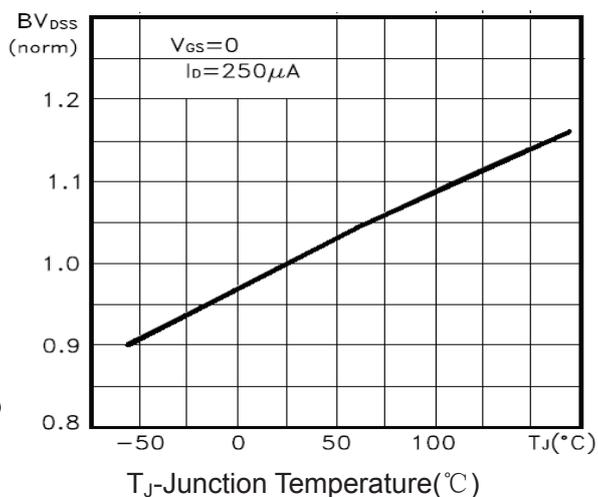


Figure 9 BV<sub>DSS</sub> vs Junction Temperature

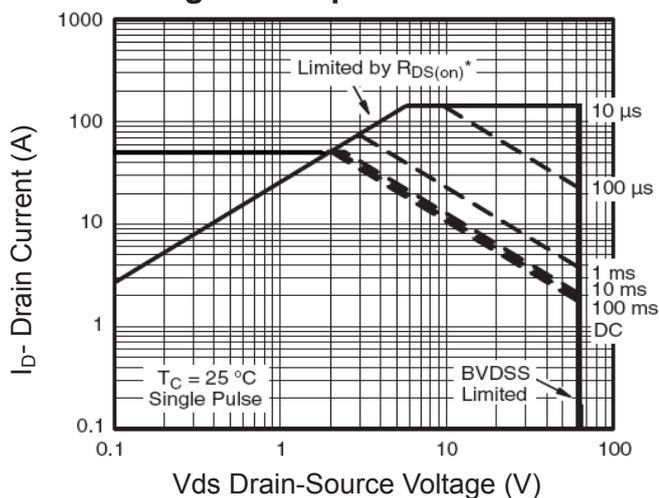


Figure 8 Safe Operation Area

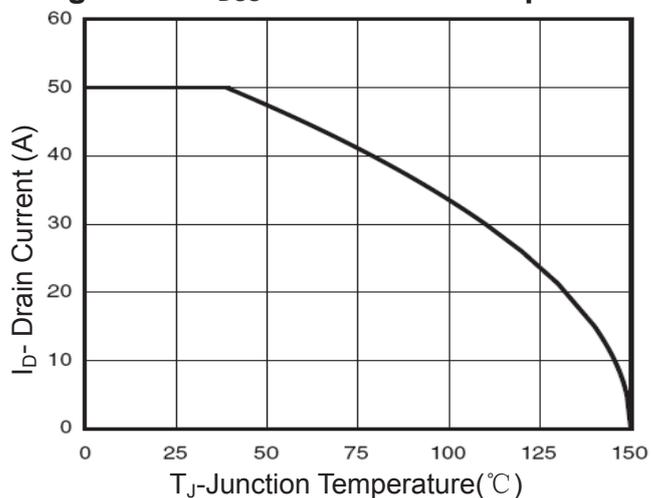


Figure 10 ID Current Derating vs Junction Temperature

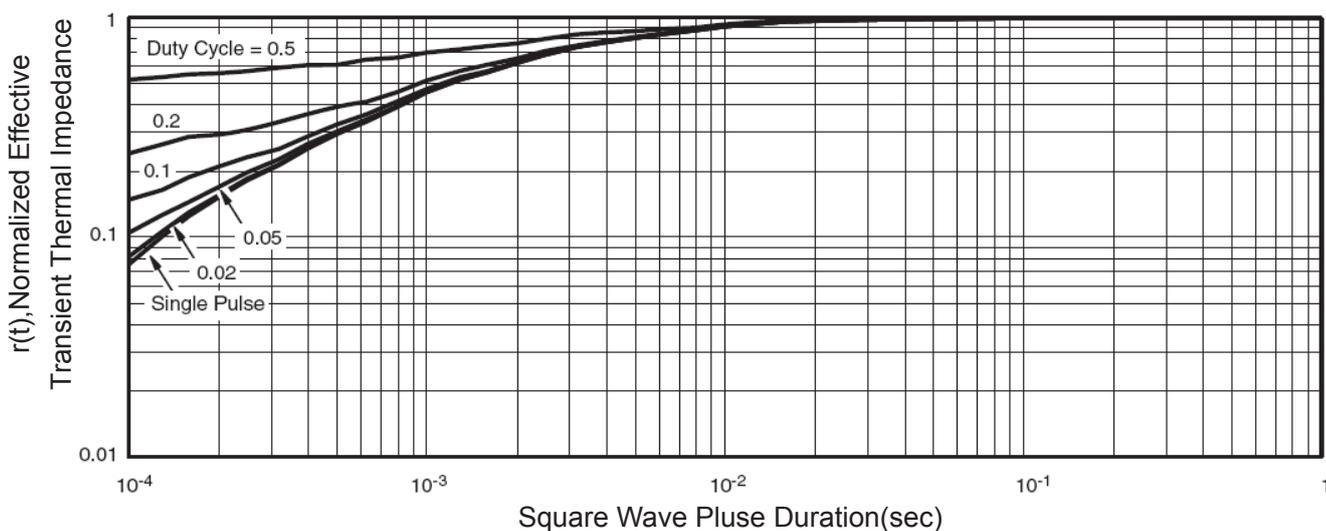
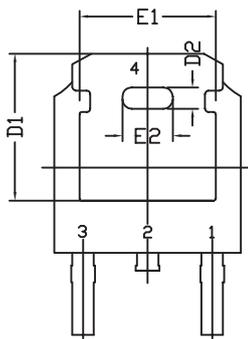
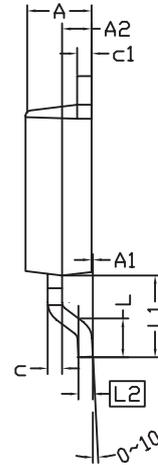
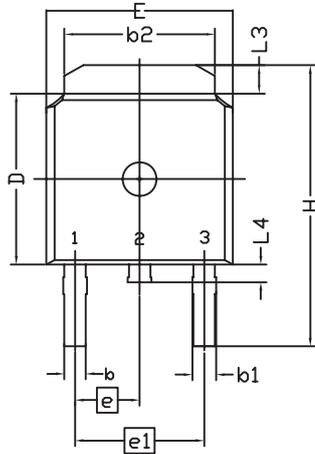


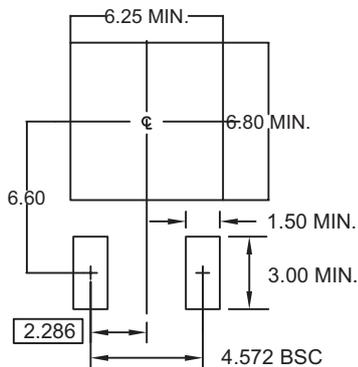
Figure 11 Normalized Maximum Transient Thermal Impedance

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T0252(DPAK) PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. DIMENSION L IS MEASURED IN GAUGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AA)

SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	-----	0.127	0.000	-----	0.005
A2	0.889	1.041	1.143	0.035	0.041	0.045
b	0.635	0.762	0.889	0.025	0.030	0.035
b1	0.762	0.840	1.143	0.030	0.033	0.045
b2	4.953	5.340	5.461	0.195	0.210	0.215
c	0.450	0.508	0.610	0.018	0.020	0.024
c1	0.450	0.508	0.610	0.018	0.020	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	5.210	5.249	5.380	0.205	0.207	0.212
D2	0.662	0.762	0.862	0.026	0.030	0.034
E	6.350	6.604	6.731	0.250	0.260	0.265
E1	4.318	4.826	4.901	0.170	0.190	0.193
E2	1.678	1.778	1.878	0.066	0.070	0.074
e	2.286 BSC			0.090 BSC		
e1	4.572 BSC			0.180 BSC		
H	9.398	10.033	10.414	0.370	0.395	0.410
L	1.270	1.520	2.032	0.050	0.060	0.080
L1	2.921 REF.			0.115REF.		
L2	0.408	0.508	0.608	0.016	0.020	0.024
L3	0.889	1.016	1.270	0.035	0.040	0.050
L4	0.635	-----	1.016	0.025	-----	0.040

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