MT1803

N-Channel Enhancement Mode Field Effect Transistor

MT Semiconductor®

http://www.mtsemi.com

Product Summary

- V_{DS}=30V
- I_D=85A(Tc=25℃, V_{GS}=10V)
- $R_{DS(ON)}$ =3.2mΩ @V_{GS}=10V,ID=25A
- $R_{DS(ON)}$ =3.8mΩ @V_{GS}=4.5V,ID=20A

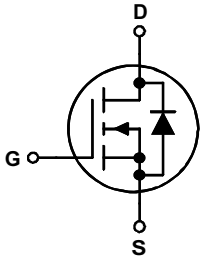
Features

- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.

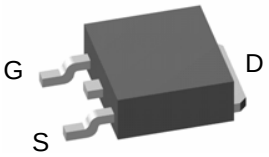
Applications

- Switching Applications.

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



D-PAK
TO-252-2L

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current	Tc=25℃	85	A
I_{DM}	Pulsed Drain Current [2]		200	A
I_S	Continuous Source Current (Diode Conduction) [1]		40	A
P_D	Maximum Power Dissipation [1]	Tc=25℃	100	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55 to 150	℃

Thermal Resistance Ratings

Symbol	Parameter	Ratings	Unit
R_{thJA}	Maximum Junction-to-Ambient	52	℃/W

Notes:

1. Surface Mounted on 1” x 1” FR4 Board, t≦10 Sec.

2. Pulse width limited by maximum junction temperature.

Electrical Characteristics (T_A=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
● Static Characteristics						
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}= 0V, I_{DS}= 250μA	30	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= 250μA	1.0	1.6	2.0	V
I_{GSS}	Gate-Body Leakage Current	V_{DS}= 0V, V_{GS}= ±20V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 24V, V_{GS}= 0V	-	-	50	μA
		V_{DS}= 24V, V_{GS}= 0V, T_J= 85℃	-	-	150	
$R_{DS(on)}$	Drain Source On State Resistance [a]	V_{GS}= 10V, I_D= 25A	-	3.2	3.9	mΩ
		V_{GS}= 4.5V, I_D= 20A	-	3.8	4.6	
V_{SD}	Diode Forward Voltage [a]	I_S= 25A, V_{GS}= 0V	-	0.5	-	V
● Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{DS}= 15V, V_{GS}= 0V, f= 1MHz	-	6200	-	pF
C_{oss}	Output Capacitance		-	690	-	
C_{rss}	Reverse Transfer Capacitance		-	255	-	
Q_g	Total Gate Charge	V_{DS}= 15V, V_{GS}= 10V, I_D= 25A	-	37	-	nC
Q_{gs}	Gate-Source Charge		-	9	-	
Q_{gd}	Gate-Drain Charge		-	5	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}= 15V, V_{GS}= 10V, I_D= 20A, R_G= 4.7Ω	-	10	-	nSec
t_r	Rise Time		-	128	-	
$T_{d(off)}$	Turn-Off Delay Time		-	44	-	
t_f	Fall Time		-	31	-	
R_g	Gate Resistance	V_{DS}= 0V, V_{GS}= 0V, f= 1MHz	-	1.9	-	Ω
t_{rr}	Source-Drain Reverse Recovery Time	I_S= 25A, di/dt= 100A/μs	-	32	-	nSec

Note:

a. Pulse test; pulse width≦300μs, duty cycle≦2%.

b. Guaranteed by design, not subject to production testing.

Typical Characteristics (Tc=25℃ unless otherwise noted)

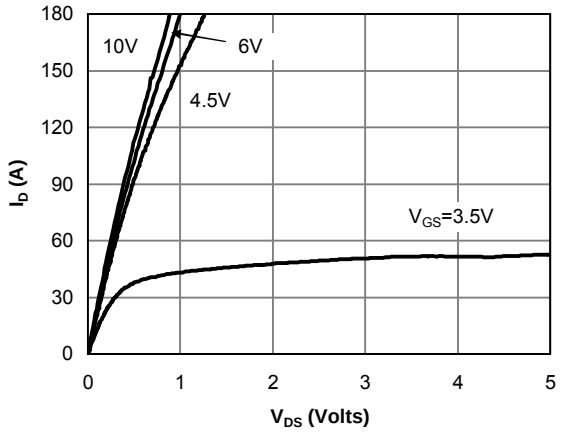


Figure 1: On-Region Characteristics

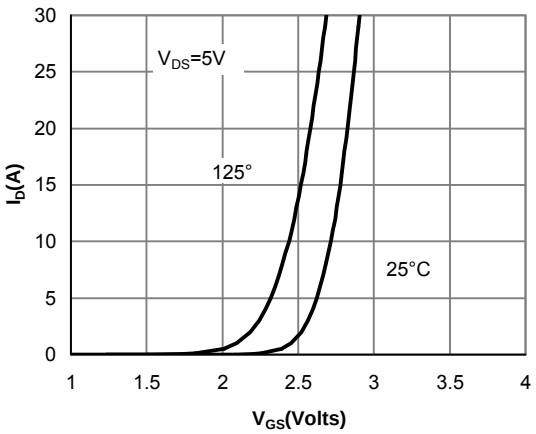


Figure 2: Transfer Characteristics

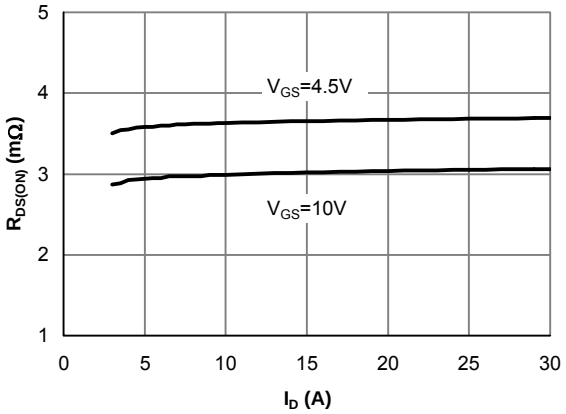


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

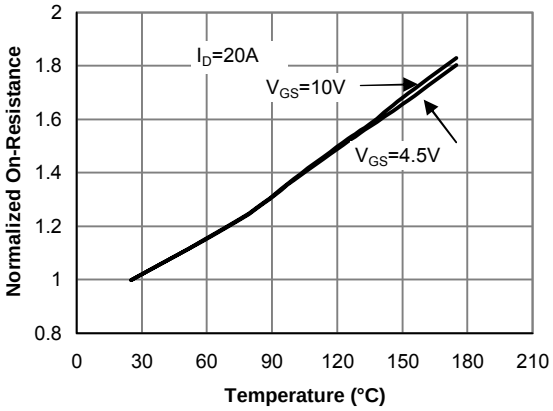


Figure 4: On-Resistance vs. Junction Temperature

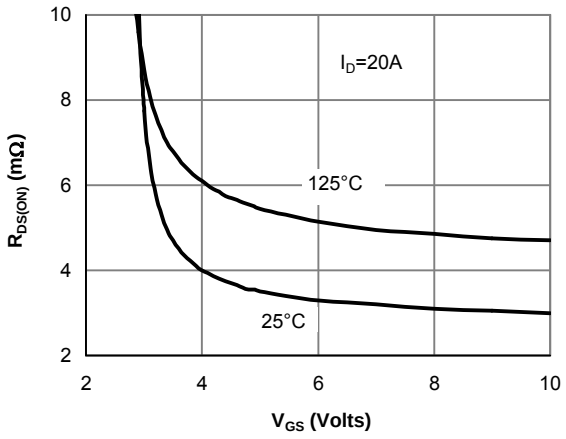


Figure 5: On-Resistance vs. Gate-Source Voltage

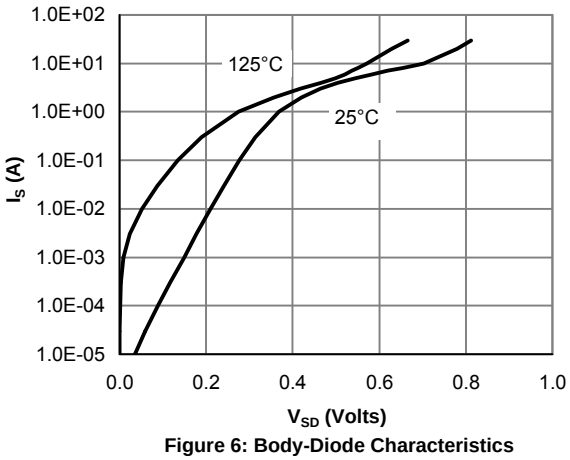


Figure 6: Body-Diode Characteristics

Typical Characteristics (Tc=25℃ unless otherwise noted)

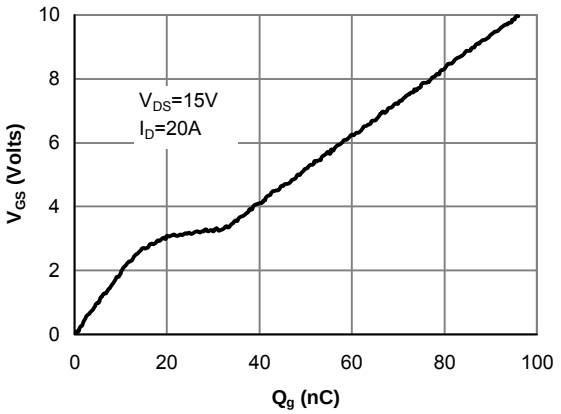


Figure 7: Gate-Charge Characteristics

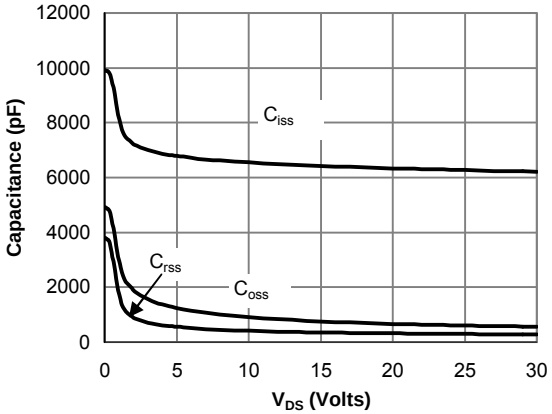


Figure 8: Capacitance Characteristics

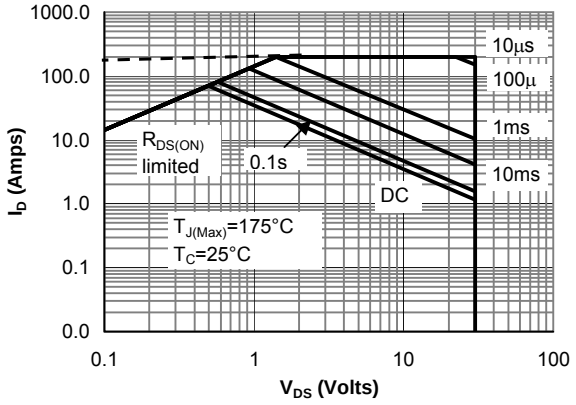


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

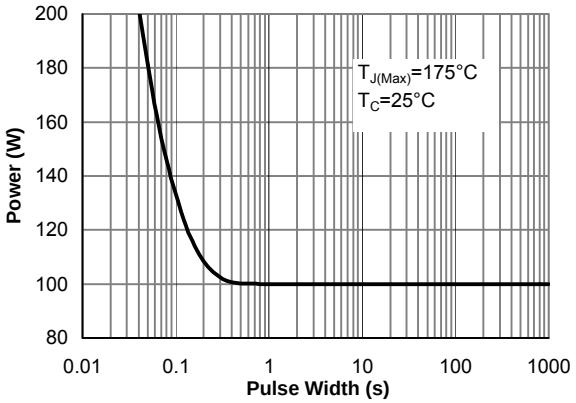


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

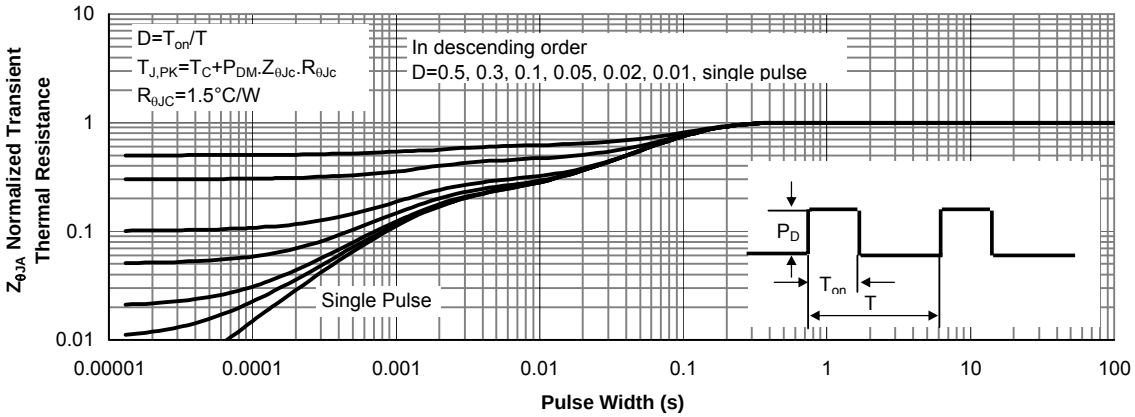


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Typical Characteristics (Tc=25℃ unless otherwise noted)

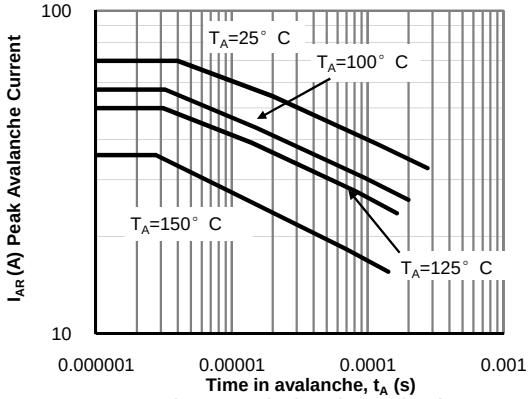


Figure 12: Single Pulse Avalanche capability (Note C)

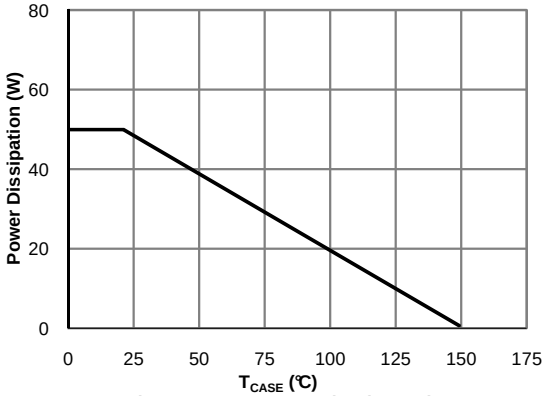


Figure 13: Power De-rating (Note F)

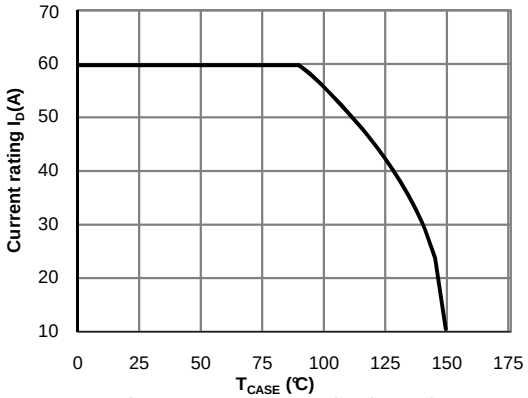


Figure 14: Current De-rating (Note F)

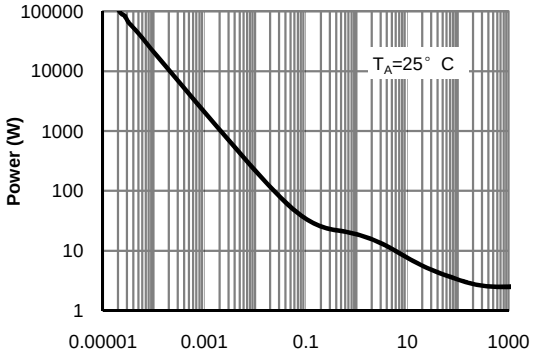


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

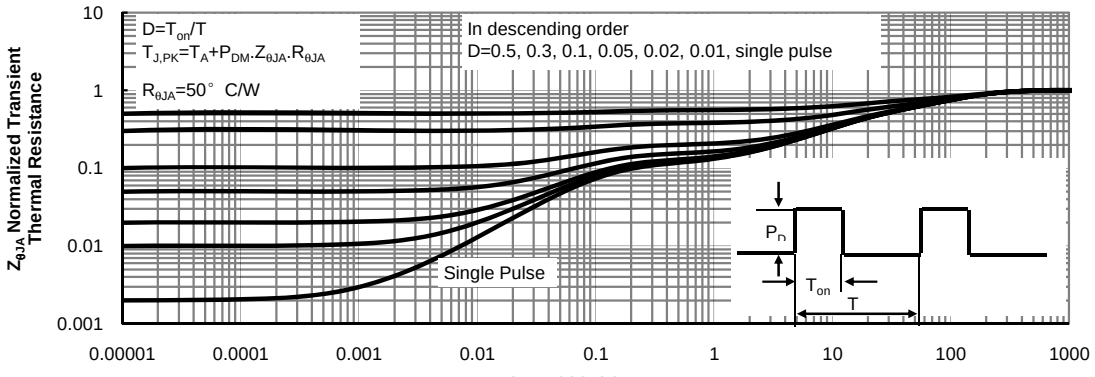
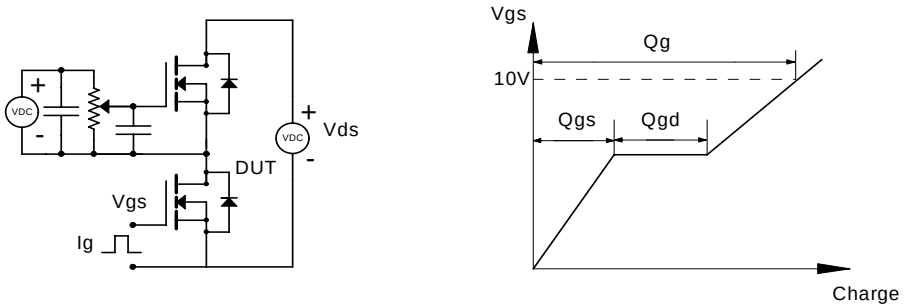
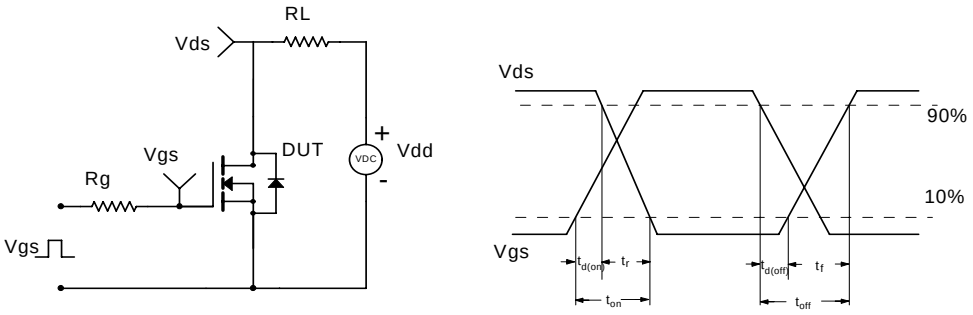


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

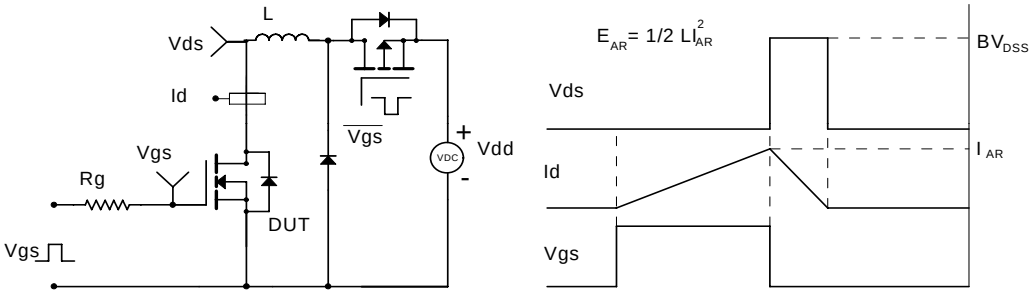
Gate Charge Test Circuit & Waveform



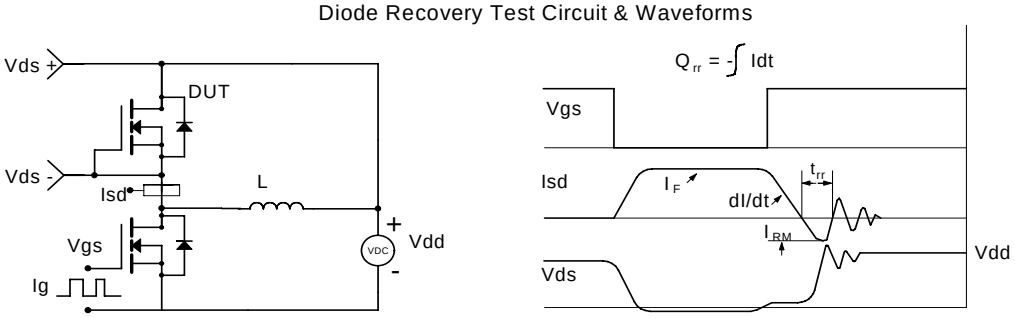
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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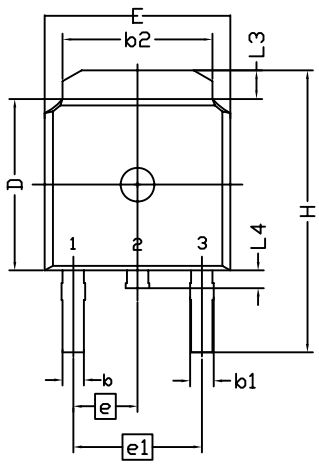
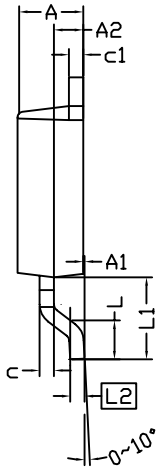
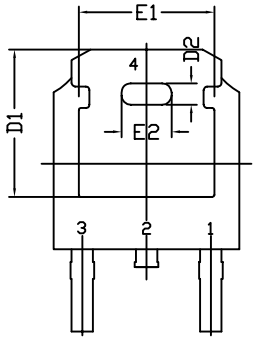
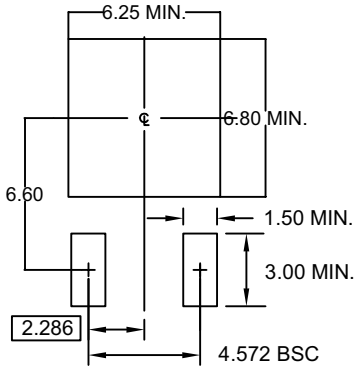
TO252(DPAK) PACKAGE OUTLINE







RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	-----	0.127	0.000	-----	0.005
A2	0.889	1.041	1.143	0.035	0.041	0.045
b	0.635	0.762	0.889	0.025	0.030	0.035
b1	0.762	0.840	1.143	0.030	0.033	0.045
b2	4.953	5.340	5.461	0.195	0.210	0.215
c	0.450	0.508	0.610	0.018	0.020	0.024
c1	0.450	0.508	0.610	0.018	0.020	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	5.210	5.249	5.380	0.205	0.207	0.212
D2	0.662	0.762	0.862	0.026	0.030	0.034
E	6.350	6.604	6.731	0.250	0.260	0.265
E1	4.318	4.826	4.901	0.170	0.190	0.193
E2	1.678	1.778	1.878	0.066	0.070	0.074
e	2.286 BSC			0.090 BSC		
e1	4.572 BSC			0.180 BSC		
H	9.398	10.033	10.414	0.370	0.395	0.410
L	1.270	1.520	2.032	0.050	0.060	0.080
L1	2.921 REF.			0.115REF.		
L2	0.408	0.508	0.608	0.016	0.020	0.024
L3	0.889	1.016	1.270	0.035	0.040	0.050
L4	0.635	-----	1.016	0.025	-----	0.040

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. DIMENSION L IS MEASURED IN GAUGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AA)

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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.